SUZAKU
Hardware Manual

Version 1.0.4

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Atmark Techno, Inc.
http://www.atmark-techno.com/

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1.About This Manual

Thank you for your purchase of the SUZAKU.

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This manual introduces the hardware specifications and methods of use of the SUZAKU.

We hope the information contained in this document will help you get the best functionality out of the SUZAKU.

2. Precautions

2.1. Safety Precautions

Before using the SUZAKU, please read the following safety precautions carefully to assure correct use.

This product uses semiconductor components designed for generic electronics equipment such as office automation equipment, communications equipment, measurement equipment and machine tools. Do not incorporate the product into devices such as medical equipment, traffic control systems, combustion control systems, safety equipment, etc. which can directly threaten human life or pose a hazard to the body or property due to malfunction or failure. Moreover, products incorporating semiconductor components can be caused to malfunction or fail due to foreign noise or surge. To ensure there will be no risk to life, the body or property even in the event of malfunction or failure, be sure to take all possible measures in the safety system design, such as using protection circuits like limit switches or fuse breakers, or system multiplexing.

2.2. Directions for Use

To avoid degradation, damage, malfunction, or fire, the following safety precautions must be observed when handing the product.

- **Input Voltage**
  Do not attempt to apply an input voltage higher than 3.3V+5%.
  Use caution in polarity.

- **Interfaces**
  Do not connect signals other than specified to each interface (external I/O, RS232C, Ethernet or JTAG).
  Use caution in polarity.
  Take care of input/output direction of signals.

- **Modification**
  Do not make modifications other than adding external I/O connectors or JTAG connectors (CON2, CON3, CON4, CON5 and CON7).

- **FPGA Programming**
  Be careful not to program the FPGA in a way that can cause a collision of peripheral circuitry (including on-board components) and a signal (i.e. output of the same signal from two devices).
  Use caution when programming the FPGA.

- **Power-on**
  Do not attempt to install or remove the FPGA I/O or JTAG connectors while power is applied to the board or peripheral circuitry.

- **Static Electricity**
  This board incorporates CMOS devices. Until using the board, store it in the provided antistatic package.

- **Latch-up**
  Due to excessive noise or a surge from the power supply or input/output, or sharp voltage fluctuations, the CMOS devices incorporated in the board can cause a latch-up. Once a latch-up occurs, this situation continues until the power supply is disconnected and thus can damage the device. It is recommended to take safety measures such as adding a protection circuit to the noise-susceptible input/output line or not sharing a power supply with devices that can be the cause of noise.

- **Impact, Vibration**
  Guard against strong impact such as a drop or collision.
  Do not put this product on anything vibrating or rotating.
  Guard against strong vibration or centrifugal force.

- **High/Low Temperatures and High Humidity**
  Do not use the product at locations subject to high/low temperatures and high humidity.

- **Dust**
  Do not use the product in dusty areas.

2.3. Precautions before Using FPGA

- **FPGA Project contained in this product**
  The FPGA project and documentation contained in this product are provided “AS IS” without warranty of any kind including any warranty of merchantability or fitness for a particular purpose, reliability, correctness or accuracy. Furthermore, Atmark Techno, Inc. does not guarantee any outcomes resulting from the use of this product.
  This product uses vendor provided tools (Xilinx’s EDK, ISE or other vendors’ tools) and IP cores to build and compile FPGA projects and to create configuration data. Atmark Techno, Inc., however, does not distribute, support or guarantee these tools.

2.4. Precautions before Using Software

- **Software contained in this product**
  The software and documentation contained in this product are provided “AS IS” without warranty of any kind including any warranty of merchantability or fitness for a particular purpose, reliability, correctness or accuracy. Furthermore, Atmark Techno, Inc. does not guarantee any outcomes resulting from the use of this product.

3. Before Getting Started

3.1. Preparations

Please make the following preparations before using the SUZAKU.

- **Development PC**
  For hardware development, prepare one PC that can run Windows 2000 or Windows XP and provides one serial port and one parallel port.
  For software development, prepare one PC that can run Linux and provides one serial port.
  For more information about software development, refer to the Software Manual.

- **D-Sub9-pin cross cable**
  Prepare one cross cable for D-Sub9-pin (female-to-female) connection.

- **D-Sub9-pin to 10-pin conversion cable**
  Prepare one D-Sub9-pin to 10-pin conversion cable for connecting the D-Sub9-pin to the pin header (10-pin) on this board.

- **The Development kit CD-ROM (hereafter called "Supplied CD-ROM")**
  This kit contains various manuals and source code relating to the SUZAKU.

- **Serial communication software**
  Serial communication software such as minicom or Tera Term is required. (Linux software can be found in the directory "tools" contained in the supplied CD-ROM).

- **DC3.3V power supply**
  Prepare one DC3.3V output power supply.

- **Xilinx ISE**
  Prepare Xilinx ISE.
  For details on Xilinx ISE, please contact a Xilinx distributor.

- **Xilinx EDK**
  Prepare Xilinx EDK.
  For details on Xilinx EDK, please contact a Xilinx distributor.

- **Xilinx Parallel Cable or equivalent**
  Prepare a parallel cable.
  For details on parallel cables, please contact a Xilinx distributor.

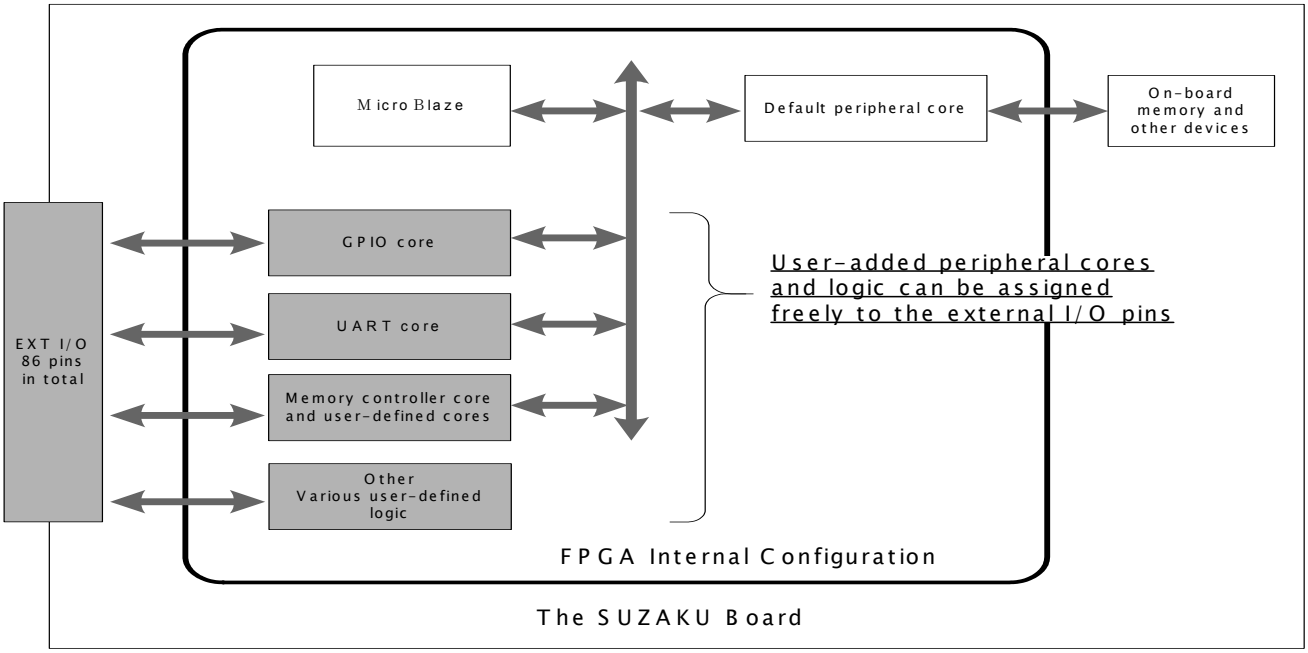
4. SUZAKU Overview

4.1. Features

The SUZAKU is a Xilinx's FPGA Spartan-3 based board computer.
It consists of a "MicroBlaze" soft processor and peripheral cores on the FPGA. It employs Linux （uCLinux） as operating system.

- **Building the Soft Processor and Peripheral Cores**
  The building of the MicroBlaze and peripheral cores utilizes Xilinx's Embedded Development Kit (EDK). The EDK enables the configuration of the MicroBlaze and peripheral cores in a GUI environment and automatically generates a netlist based on the configuration information.

- **Customization**
  The interior of the FPGA is designed for user-customization.
  The board is equipped with 86 external I/O pins that can be used at user's disposal.
  For instance, you can easily customize the board to increase the number of PIOs or UARTs by assigning these external I/O pins to them.



* You will need Xilinx's EDK and ISE to customize the FPGA. They can be obtained directly from Xilinx or through Xilinx's local distributors.

- **LAN**
  The board is equipped with a LAN (10Base-T/100Base-Tx) port for off-the-shelf LAN cable (UTP) connections.

- **Operating System**
  The board employs µCLinux as its standard operating system. It allows the use of a GNU assembler or C compiler in the development of application software.
  The board comes with a LAN controller device driver and protocols for easy network connection.
  For details on the operating system, refer to the Software Manual.

4.2. Specifications

The main specifications of this board are shown in Table 4-1.

Table 4-1 SUZAKU Specifications

FPGA	Xilinx Spartan-3 (XC3S400 FT256)
Soft Processor	MicroBlaze
Crystal Oscillator	3.6864MHz (frequency multiplied by FPGA's internal DCM)
Memory	BRAM 8Kbyte FLASH Memory 4Mbyte SDRAM 16Mbyte
Configuration	Stored in FLASH Memory, Controller TE7720
JTAG	2 ports (FPGA, TE7720)
Ethernet	10Base-T/100Base-Tx
Serial	UART 115.2kbps
Timer	2ch (1ch for OS)
Free I/O Pin	86-pin
Reset Function	Software Reset
Power Supply	Voltage: 3.3V±3% Consumption current: 350mA typ (while processor is operating)
Dimensions	72×47mm

4.3. Block Diagram

The entire block diagram of the SUZAKU is shown in Figure 4-1.
This is the minimum configuration needed to run uCLinix.

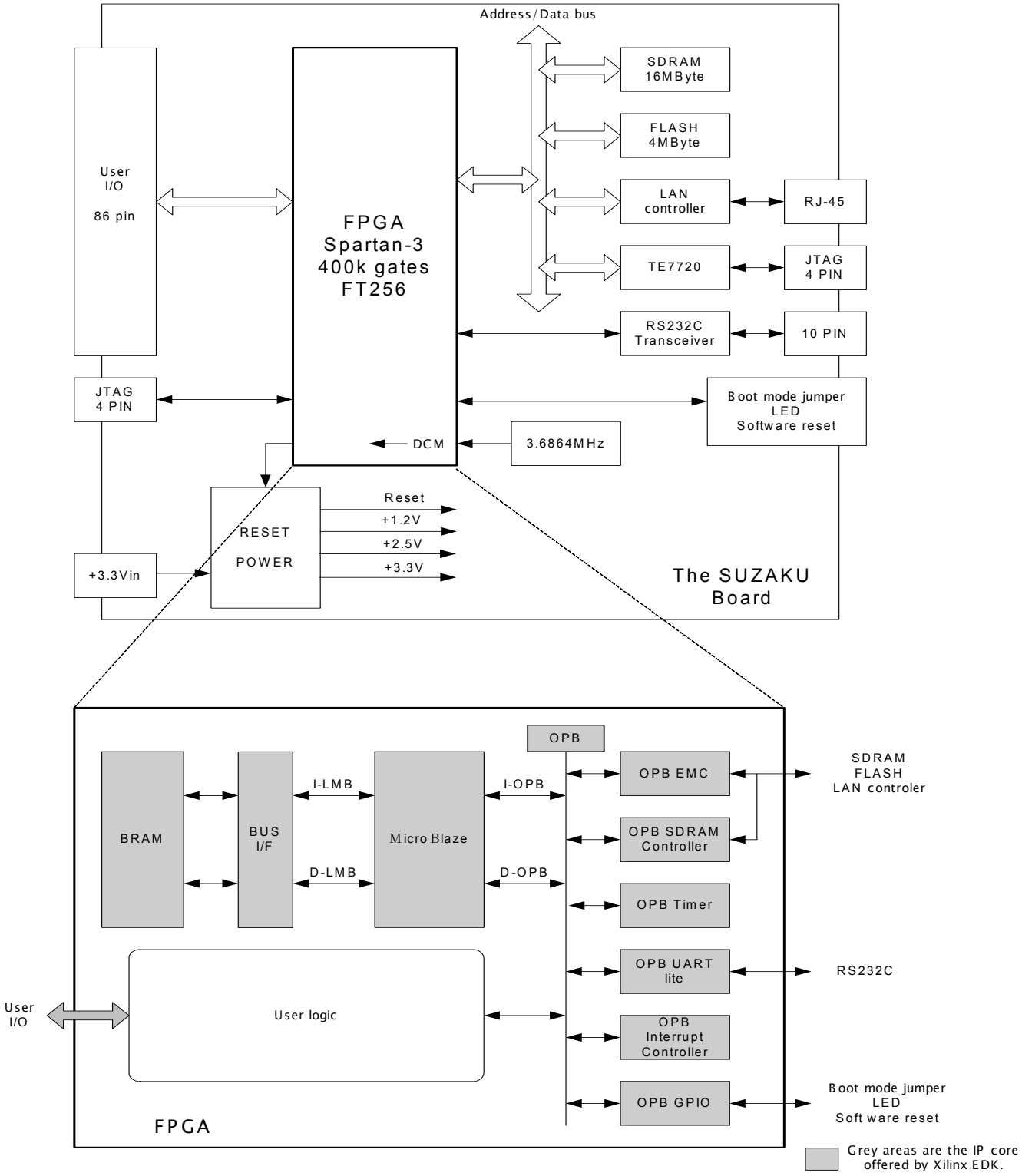


Figure 4-1 Block Diagram of SUZAKU

4.4. Functions

4.4.1. Processor

The board uses the MicroBlaze in the FPGA. The overview of MicroBlaze is as follows:

- 32-bit, RISC Processor
- 32-bit, fixed length instruction
- 32 generic 32bit registers
- 3-Stage Pipeline
- Instruction cache and data cache
- Hardware multiplier
- Hardware debug logic supported

4.4.2. Bus

The bus consists of the following three bus types.

- FPGA Internal LMB
  A dedicated bus used to connect the MicroBlaze and BRAM (FPGA internal memory).
- FPGA Internal OPB
  A bus used to connect multiple peripheral IP cores.
  When customizing, peripheral cores are added to this bus.
- FPGA External Bus
  A bus used to connect external memory devices through OPB EMC and OPB SDRAM.

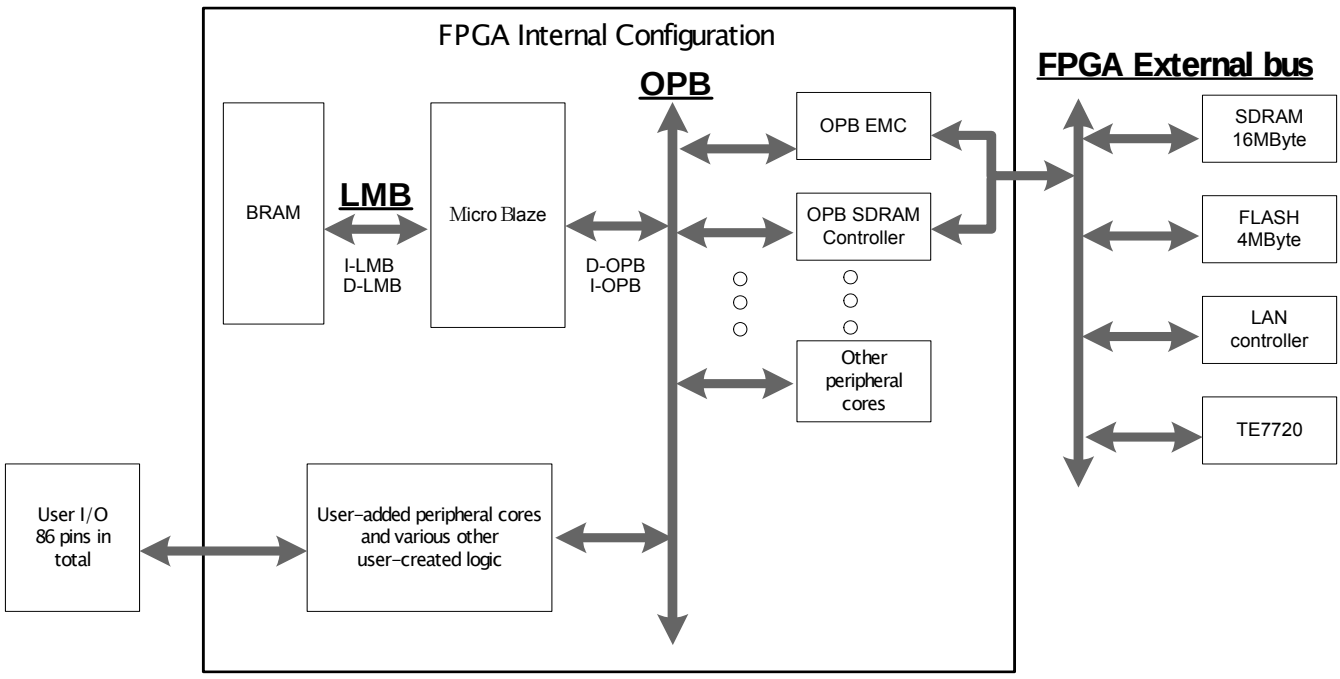


Figure 4-2 SUZAKU Bus Configuration

4.4.3. Memory

Memory consists of the following three types.

- FPGA Internal BRAM (Default 8KByte)
  This memory is used for the boot program.
  After booting, it can be used for user programs except for the first 32 bytes (interrupt vector area).
- FPGA External FLASH Memory 4MByte
  This memory is used to store data such as a high performance boot loader, the Linux system and FPGA configurations.
  It is connected to OPB through OPB EMC.
- FPGA External SDRAM 16MByte
  This memory is used as the main memory for Linux.
  It is connected to OPB through OPB SDRAM.

4.4.4. Interrupt

The OPB INTC in the FPGA is used as the OS interrupt controller.

4.4.5. Timer

The OPB Timer in the FPGA is used as the OS timer.

4.4.6. Serial Console

The OPB UART Lite in the FPGA is used as the OS serial console.
The OPB UART Lite is connected to the connector (CON1) through the RS232C transceiver.
The RS232C transceiver is the 4-channel version. The first two channels are used for OS serial console operation and the remaining two channels are unused. Using these unused channels, you can connect GPIO or user logic for flow control or connect another OPB UART Lite as the secondary UART port.

- Serial console settings:
  Transfer Rate: 115.2kbps
  Data: 8bit
  Stop Bit: 1bit
  Flow Control: Not supported

4.4.7. LAN

SMSC's LAN91C113 is employed as the LAN controller, external to the FPGA.
The LAN91C113 is connected to OPB via OPB EMC.
The LAN controller is also equipped with a RJ-45 connector for LAN cable connection (UTP).

4.4.8. External I/O

The board provides 86 external I/O pins that can be used freely by the user (CON2、CON3、C0N4 and CON5).
(Note that on-board connectors are not provided).
All the external I/Os are directly connected to the FPGA's free I/O pin.
The power for the FPGA I/O (VCCO) is supplied from the internal logic power supply +3.3V.
For the rated value of I/O voltage and driving current, refer to the Spartan-3 data sheet.

Due to the sequence and delay circuits, the internal logic power supply +3.3V takes up to 20msec to start-up. To avoid latch-up, all the devices connecting to the external I/O must use the internal logic power output +3.3V of this board (refer to Section 4.4.15 "Internal Logic Power Output +3.3V") otherwise a buffer device will be required.

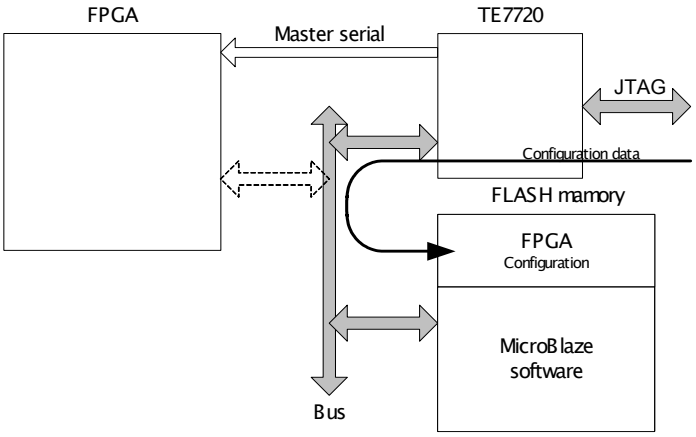
4.4.9. FPGA Configuration

The TE7720 (developed by Tokyo Electron Device Limited) is used as the FPGA configuration IC.
The TE7720 is an IC that programs data sent from the JTAG(CON2) into the FLASH memory and reads it to configure the FPGA when the board is restarted (Figure 4.3).

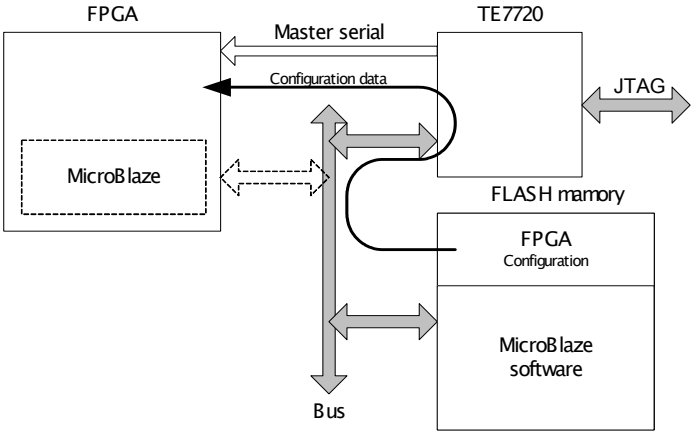
The whole FLASH memory area can be read and written from the processor.
Write the Linux system or FPGA configuration data received via LAN or RS232C into the FLASH memory, reboot the system, and the board will start to operate as a new version of board with different functionality.
Moreover, the SUZAKU is equipped with a reset circuit that can be controlled by software, enabling remote reconfiguration.

You can get the free software (LBPLAY2.EXE) for transferring data from JTAG(CON2) to TE7720 by downloading it from the Tokyo Electron Device home page (the software is also contained in the provided CD-ROM).
For information on configuration, refer to **Section 10 "FPGA Configuration"**.

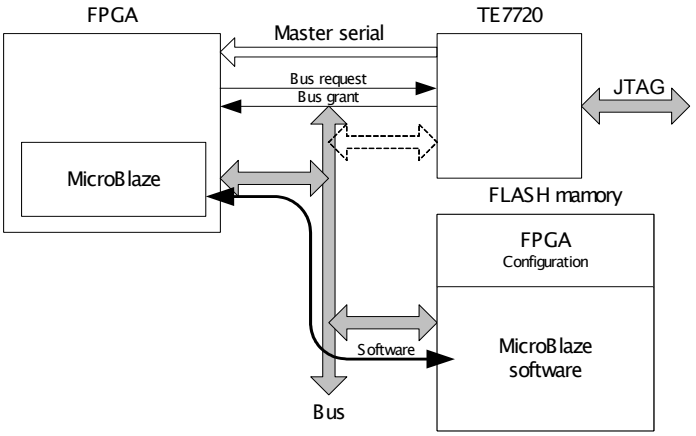
If incorrect data was programmed to the FPGA or an error occurred while programming, do not run the SUZAKU. Collision between signals and the FPGA external circuit components (including on-board componenst) or abnormal operation could cause thermal degradation or damage. To avoid this, once switch off the power, short "JP2" and perform a reprogramming.
When the power is turned on again and "JP2" is shorted, the SUZAKU will stop the FPGA configuration to allow reprogramming.



Writing to Flash memory via the TE7720



Configuration of the FPGA via the TE7720 from Flash memory at power-up

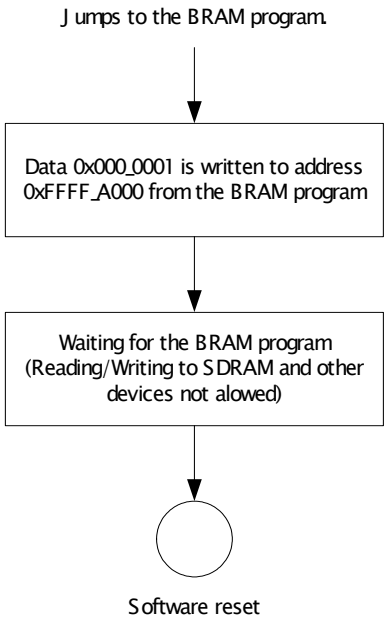


The MicroBlaze utilizes flash memory after the FPGA configuration completes

Figure 4-3 FPGA Configuration

4.4.10. Software Reset Function

When the software reset is performed, the board reads the configuration data from the flash memory. It then executes the FPGA configuration and outputs the reset signal to each device IC.
The software reset can be performed either by using the Linux reboot command or writing the data, 0x000_0001, at the address of 0xFFFF_A000 directly from the BRAM program. In the case that the software reset is performed directly from the BRAM program, be careful not to read or write to SDRAM or other devices (including executing programs).



Software reset directly from the BRAM program

4.4.11. JTAG

The board provides the following two types of JTAG.

- **JTAG Connector for FPGA Programming (CON2)**
  This JTAG connector is used to program the FPGA configuration data to the Flash memory.
  (The connector is not mounted on the board)
  Connect a JTAG cable such as Xilinx's Parallel Cable to the connector (CON2) to perform programming using the proprietary software (LBPLAY2.EXE).
  The I/O voltage of this JTAG is +3.3V. So please use a JTAG cable compatible with the +3.3V output.
  TMS, TDI and TCK are all pulled up to +3.3V within the board via 4.7kΩ.
  For information on configuration, refer to **Section 10 "FPGA Configuration"**.
- **JTAG Connector for FPGA (CON7)**
  This is a JTAG connector for the FPGA (connector not mounted).
  The connector is directly connected to the JTAG pins of the FPGA.
  The I/O voltage of this JTAG is +2.5V. So please use a JTAG cable compatible with the +2.5V output.
  TMS, TDI and TCK are all pulled up to +2.5V within the board via 4.7kΩ.

4.4.12. Setting Jumpers

The following two types of setting jumpers are available.

- **Boot Mode Jumper (JP1)**

  This jumper is used to switch the boot mode.
  If it is set to open, the board will auto-boot.
  If it is set to short, the board will go into boot loader mode.
  (For more information about the boot-up mode, refer to the software manual)

- **FPGA Programming Jumper (JP2) – connected to F3 of Spartan-3**

  This jumper is used to program configuration data from the FPGA Programming JTAG to the Flash memory.
  If it is set to open, the board will boot normally.
  If it is set to short, the board will program the FPGA configuration data to the Flash memory.
  For more information on configuration, refer to **Section 10 "FPGA Configuration."**
  (When this jumper is shorted at power on, FPGA configuration will be halted to allow programming to Flash memory)

4.4.13. LED

There are the two following types of LEDs.

- **Power-on LED Green (D3)**

  This LED will light when 3.3V is supplied to the board.

- **User Control LED Red (D1) – connected to G5 of Spartan-3**

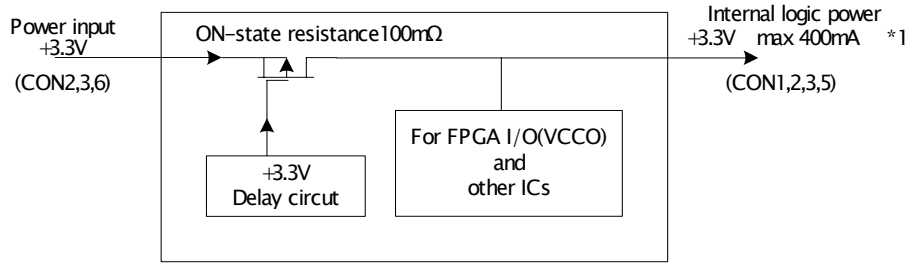
  This LED is user-controllable.
  It will light at "LO." level.
  It is connected to the FPGA.

4.4.14. Power Input +3.3V

Power can be fed to the board from either of the "+3.3V Power Inputs" at CON2, CON3 and CON6.
The +3.3V must be ±3% in accuracy and simple increment.
Do not repeatedly turn the board on-and-off at very short time intervals.
The input is equipped with laminated ceramic condenser 10μF.

4.4.15. Internal Logic Power Output +3.3V

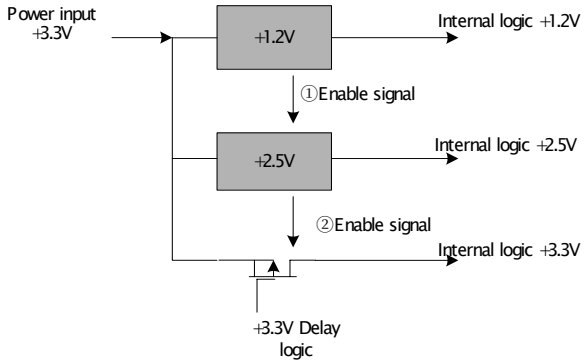
The internal logic power output +3.3V is a power supply used to feed +3.3V to I/O (VCCO) of the FPGA and other ICs.
Up to 400mA [*1] can be supplied to the external devices from CON1, CON2, CON3 and CON5.
However, due to significantly large load variation on the external devices, voltage variation can occur depending on the response of the power input +3.3V.

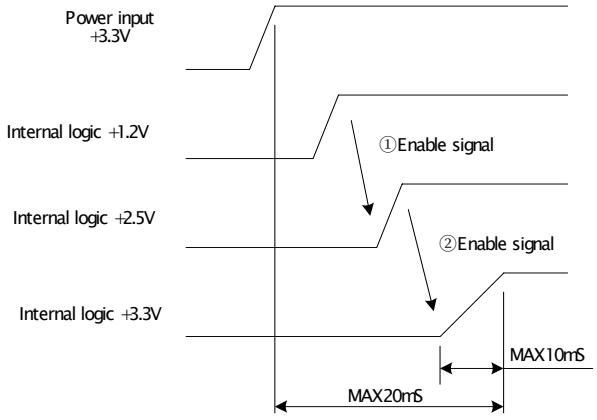


*1 If signals are sent from the external I/O, total maximum current is given by
Total Maximum Current = 400mA – Output Current of External I/O Signal

4.4.16. Internal Power Supply Sequence

The internal power supply boots up in the following sequence.





5. Memory Map

5.1. SUZAKU Memory Map

The memory map of the board is shown in Table 5-1.
It is the minimum configuration required to run uCLinux.

Table 5-1 SUZAKU Memory Map

Start Address	End Address	Peripheral	Device
0x0000 0000	0x0000 1FFF	BRAM	
0x0000 1000	0x7FFF FFFF	Reserved	
0x8000 0000	0x80FF FFFF	OPB-SDRAM Controller	SDRAM 16MByte
0x8100 0000	0xFEFF FFFF	Free	
0xFF00 0000	0xFF7F FFFF	OPB-EMC	FLASH Memory 4MByte
0xFF80 0000	0xFFCF FFFF	Free	
0xFFE0 0000	0xFFEF FFFF	OPB-EMC	LAN Controller
0xFFF0 0000	0xFFFF 0FFF	Free	
0xFFFF 1000	0xFFFF 10FF	OPB-Timer	
0xFFFF 1100	0xFFFF 1FFF	Free	
0xFFFF 2000	0xFFFF 20FF	OPB-UART Lite	RS232C
0xFFFF 2100	0xFFFF 2FFF	Free	
0xFFFF 3000	0xFFFF 30FF	OPB-Interrupt Controller	
0xFFFF 3100	0xFFFF 9FFF	Free	
0xFFFF A000	0xFFFF A0FF	OPB-GPIO	Boot Mode Jumper LED Software Reset
0xFFFF A100	0xFFFF FFFF	Free	

6. FPGA Pin Assignment

Table 6-1 shows all the pin assignments of the FPGA (Xilinx Spartan-3　XC3S400 FT256).

Table 6-1　FPGA Pin Assignment　External I/O (1/3)

No.	Bank	Signal Name	I/O	Function	Connected to
A5	0	IOa_0	I/O	External I/O	CON2 (refer to Section 7)
A7	0	IOb_0	I/O	〃	〃
A3	0	IO/VREF0P	I/O	〃	〃
D5	0	IO/VREF0N	I/O	〃	〃
B4	0	01N_0/VRP_0	I/O	〃	〃
A4	0	01P_0/VRN_0	I/O	〃	〃
C5	0	25N_0	I/O	〃	〃
B5	0	25P_0	I/O	〃	〃
E6	0	27N_0	I/O	〃	〃
D6	0	27P_0	I/O	〃	〃
C6	0	28N_0	I/O	〃	〃
B6	0	28P_0	I/O	〃	〃
E7	0	29N_0	I/O	〃	〃
D7	0	29P_0	I/O	〃	〃
C7	0	30N_0	I/O	〃	〃
B7	0	30P_0	I/O	〃	〃
D8	0	31N_0	I/O	〃	〃
C8	0	31P_0/VREF0	I/O	〃	〃
B8	0	32N_0/GCLK7	I/O	〃	〃
A8	0	32P_0/GCLK6	I/O	〃	〃
A9	1	IOa_1	I/O	〃	〃
A12	1	IOb_1	I/O	〃	〃
C10	1	IOc_1	I/O	〃	〃
D12	1	IO/VREF1	I/O	〃	〃
A14	1	01N_1/VRP_1	I/O	〃	〃
B14	1	01P_1/VRN_1	I/O	〃	〃
A13	1	10N_1/VREF1	I/O	〃	〃
B13	1	10P_1	I/O	〃	〃
B12	1	27N_1	I/O	〃	〃
C12	1	27P_1	I/O	〃	〃
D11	1	28N_1	I/O	〃	〃
E11	1	28P_1	I/O	〃	〃

Table 6-2　FPGA Pin Assignment　External I/O (2/3)

No.	Bank	Signal Name	I/O	Function	Connected to
B11	1	29N_1	I/O	External I/O	CON3 (Refer to Section 7)
C11	1	29P_1	I/O	〃	〃
D10	1	30N_1	I/O	〃	〃

E10	1	30P_1	I/O	〃	〃
A10	1	31N_1/VREF1	I/O	〃	〃
B10	1	31P_1	I/O	〃	〃
C9	1	32N_1/GCLK5	I/O	〃	〃
D9	1	32P_1/GCLK4	I/O	〃	〃
G16	2	Oa_2	I/O	〃	〃
B16	2	16P_2	I/O	〃	〃
C16	2	17N_2	I/O	〃	〃
C15	2	17P_2/VREF2	I/O	〃	〃
D14	2	19N_2	I/O	〃	〃
D15	2	19P_2	I/O	〃	〃
D16	2	20N_2	I/O	〃	〃
E13	2	20P_2	I/O	〃	〃
E14	2	21N_2	I/O	〃	〃
E15	2	21P_2	I/O	〃	〃
E16	2	20P_2	I/O	〃	〃
F12	2	21N_2	I/O	〃	〃
F13	2	21P_2	I/O	〃	〃
F14	2	22N_2	I/O	〃	〃
F15	2	22P_2	I/O	〃	〃
G12	2	23N_2/VREF2	I/O	〃	〃
G13	2	23P_2	I/O	〃	〃
G14	2	24N_2	I/O	〃	〃
G15	2	24P_2	I/O	〃	〃
H13	2	39N_2	I/O	〃	〃
H14	2	39P_2	I/O	〃	〃
H15	2	40N_2	I/O	〃	〃
H16	2	40P_2/VREF2	I/O	〃	〃
K15	3	IOa_3	I/O	〃	〃
P16	3	01N_3/VRP_3	I/O	〃	〃
R16	3	01P_3/VRN_3	I/O	〃	〃

Table 6-3 FPGA Pin Assignment External I/O (3/3)

No.	Bank	Signal Name	I/O	Function	Connected to
P15	3	16N_3	I/O	External I/O	CON5 (Refer to Section 7)
P14	3	16P_3	I/O	〃	〃
N16	3	17N_3	I/O	〃	〃
N15	3	17P_3/VREF3	I/O	〃	〃
M14	3	19N_3	I/O	〃	〃
N14	3	19P_3	I/O	〃	〃
M16	3	20N_3	I/O	〃	〃
M15	3	20P_3	I/O	〃	〃
L13	3	21N_3	I/O	〃	〃
M13	3	21P_3	I/O	〃	〃
L15	3	22N_3	I/O	〃	〃
L14	3	22P_3	I/O	External I/O	CON4 (Refer to Section 7)

K12	3	23N_3	I/O	〃	〃
L12	3	23P_3/VREF3	I/O	〃	〃
K14	3	24N_3	I/O	〃	〃
K13	3	24P_3	I/O	〃	〃
J14	3	39N_3	I/O	〃	〃
J13	3	39P_3	I/O	〃	〃
J16	3	40N_3/VREF3	I/O	〃	〃
K16	3	40P_3	I/O	〃	〃

Table 6-4 FPGA Pin Assignment - Internal Device (1/3)

No.	Bank	Signal Name	I/O	Function	Connected to
T12	4	LA(22)	O	FPGA external address bus	SDRAM, FLASH memory and LAN controller
T14	4	LA(21)	O	〃	〃
N12	4	LA(20)	O	〃	〃
P13	4	LA(19)	O	〃	〃
T10	4	LA(18)	O	〃	〃
R13	4	LA(17)	O	〃	〃
T13	4	LA(16)	O	〃	〃
P12	4	LA(15)	O	〃	〃
R12	4	LA(14)	O	〃	〃
M11	4	CFG_DATA	I	Configuration data	TE7720
N11	4	LA(13)	O	FPGA external address bus	SDRAM, FLASH memory, LAN controller
P11	4	LA(12)	O	〃	〃
R11	4	LA(11)	O	〃	〃
M10	4	LA(10)	O	〃	〃
N10	4	LA(9)	O	〃	〃
P10	4	LA(8)	O	〃	〃
R10	4	SYS_CLK_OUT	O	Clock output to SDRAM	SDRAM
N9	4	CFG_INIT*	I	Configuration INIT	TE7720, JP2
P9	4			Unused	
R9	4	RAM_CLK	I	Clock DCM feedback input for SDRAM	SDRAM
T9	4	SYS_CLK_IN	I	System clock input	Oscillator 3.6864MHz
N5	5	LA(7)	O	FPGA external address bus	SDRAM, FLASH memory, LAN controller
P7	5	LA(6)	O	〃	〃
T5	5	LA(5)	O	〃	〃
T8	5	LA(4)	O	〃	〃
T3	5	LA(3)	O	〃	〃
R3	5	LA(2)	O	〃	〃
T4	5	LA(1)	O	〃	〃
R4	5	LA(0)	O	〃	〃
R5	5	LD(15)	I/O	FPGA external data bus	SDRAM, FLASH memory, LAN controller
P5	5	LD(14)	I/O	〃	〃
N6	5	LD(13)	I/O	〃	〃
M6	5	LD(12)	I/O	〃	〃
R6	5	LD(11)	I/O	〃	〃

Table 6-5 FPGA Pin Assignment – Internal Device (2/3)

No.	Bank	Signal Name	I/O	Function	Connected to
P6	5	LD(10)	I/O	〃	〃
N7	5	LD(9)	I/O	〃	〃
M7	5	LD(8)	I/O	〃	〃
T7	5	LD(7)	I/O	〃	〃
R7	5	LD(6)	I/O	〃	〃
P8	5			Unused	
N8	5			Unused	
K1	6	LDA(5)	I/O	FPGA external data bus	SDRAM, FLASH memory, LAN controller
R1	6	LD(4)	I/O	〃	〃
P1	6	LD(3)	I/O	〃	〃
P2	6	LD(2)	I/O	〃	〃
N3	6	LD(1)	I/O	〃	〃
N2	6	LD(0)	I/O	〃	〃
N1	6	BUS_REQ	O	Bus request	TE7720
M4	6	BUS_REL	I	Bus Capture	TE7720
M3	6	RAM_CS*	O	SDRAM CS	SDRAM
M2	6	RAM_RAS*	O	SDRAM RAS	〃
M1	6	RAM_CAS*	O	SDRAM CAS	〃
L5	6	RAM_WE*	O	SDRAM WE	〃
L4	6	RAM_CKE	O	SDRAM CKE	〃
L3	6	RAM_UQDM	O	SDRAM UQDM	〃
L2	6	RAM_LQDM	O	SDRAM LQDM	〃
K5	6	RAM_BS1	O	SDRAM BS	〃
K4	6	RAM_BS0	O	SDRAM BS	〃
K3	6	FLASH_CE*	O	FLASH memory CE	FLASH memory
K2	6	FLASH_OE*	O	FLASH memory OE	〃
J4	6	FLASH_WE*	O	FLASH memory WE	〃
J3	6	FLASH_BYTE*	O	FLASH memory BYTE*	〃
J2	6	FLASH_R_B	I	FLASH memory R/B	〃
J1	6	MAC_BE1*	O	LAN controller BE1	LAN controller
G2	7	MAC_BE0*	O	LAN controller BE0	〃
C1	7	MAC_AEN	O	LAN controller AEN	〃
B1	7	MAC_RD*	O	LAN controller RD	〃
C2	7	MAC_WR*	O	LAN controller WR	〃
C3	7	MAC_ARDY	I	LAN controller ARDY	〃
D1	7	MAC_ ADS*	O	LAN controller ADS	〃
D2	7	MAC_INTR	I	LAN controller INTR	〃
E3	7			Unused	
D3	7			Unused	
E1	7	CNSL_CTS*	I	Console CTS	RS232C transceiver to CON1 (Refer to Section 7)
E2	7	CNSL_RXD	I	Console RXD	〃
F4	7	CNSL_RTS	O	Console RTS	〃
E4	7	CNSL_TXD	O	Console TXD	“

Table 6-6 FPGA Pin Assignment – Internal Devices (3/3)

No.	Bank	Signal Name	I/O	Function	Connected to
F2	7	FPGA_RESET_EN	O	Self reset output	Reset circuit
F3	7	BOOTMODE	I	Boot mode detection	JP1 (Refer to Section 7)
G5	7	LED*	O	User control LED	D1 (Refer to Section 7)
F5	7	SYS_RST_IN	I	System reset input	Reset circuit
G3	7			Unused	
G4	7			Unused	
H3	7			Unused	
H4	7			Unused	
H1	7			Unused	
G1	7			Unused	

Table 6-7 FPGA Pin Assignment – JTAG, Configuration

No.	Bank	Signal Name	I/O	Function	Connected to
C14		TCK	I	JTAG	CON7 (Refer to Section 7)
A2		TDI	I	JTAG	〃
A15		TDO	O	JTAG	〃
C13		TMS	I	JTAG	〃
T15		CFG_CLK	O	Configuration CLK	TE7720
B3		PROG_B	I	Configuration PROG_B	Reset circuit
R14		CFG_DONE	O	Configuration DONE	TE7720
C4		HSWAP_EN		Open	
P3		M0	I	Configuration mode	Ground
T2		M1	I	Configuration mode	Ground
P4		M2	I	Configuration mode	Ground

7. Interface Specifications

7.1. Interface Layout

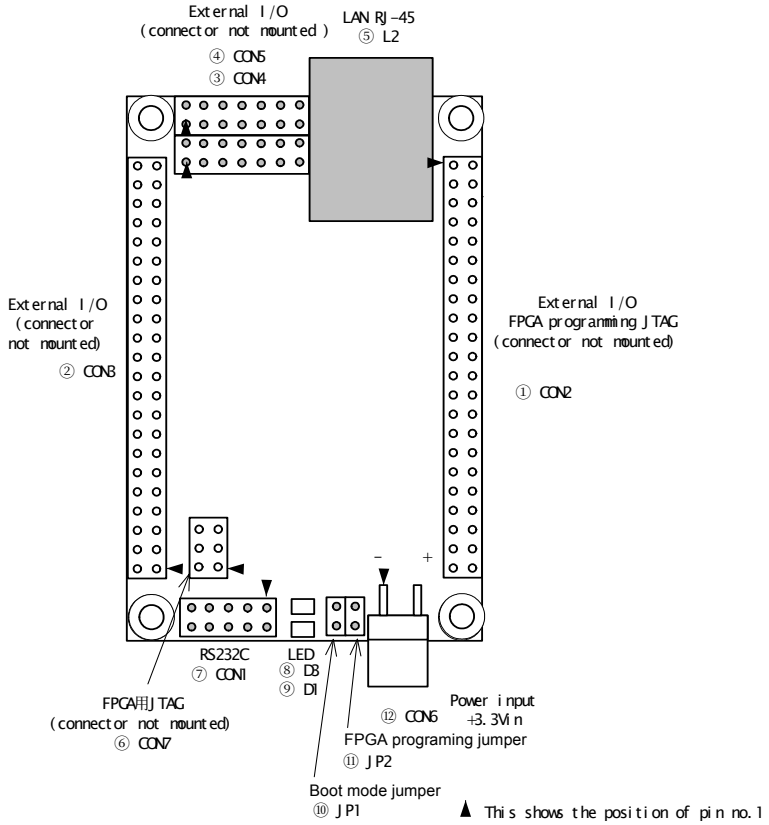


Figure 7-1 Layout of Interfaces

Table 7-1 Interface Details

	Part Number	Description
1	CON2	External I/O, JTAG connector for FPGA programming Total I/Os 32PIN
2	CON3	External I/O connector Total I/Os 34PIN
3	CON4	External I/O connector Total I/Os 10PIN
4	CON5	External I/O connector Total I/Os 10PIN
5	L2	Ethernet 10/100 Base-T connector
6	CON7	FPGA JTAG connector
7	CON1	RS232C connector
8	D3	Power on LED (Green)
9	D1	User Control LED (Red)
10	JP1	Boot mode jumper
11	JP2	Jumper for FPGA programming
12	CON6	Power input +3.3V connector

7.2. CON2 External I/O, FPGA Programming JTAG Connector

This JTAG connector is used for external I/O or FPGA programming (connector not mounted on the board).

Table 7-2 CON2 Connector for External I/O or FPGA Programming

No.	Signal Name	I/O	Function
1	GND		Ground
2	+3.3VOUT		Power output for internal logic +3.3V
3	CFG_TCK		JTAG for FPGA programming TCK
4	CFG_TDI		" TDI
5	CFG_TDO		" TDO
6	CFG_TMS		" TMS
7	IOa_0		External I/O pin number Spartan-3 connection A5
8	IOb_0		" A7
9	IO/VREF0P		" A3
10	IO/VREF0N		" D5
11	01N_0/VRP_0		" B4
12	01P_0/VRN_0		" A4
13	25N_0		" C5
14	25P_0		" B5
15	27N_0		" E6
16	27P_0		" D6
17	28N_0		" C6
18	28P_0		" B6
19	GND		Ground
20	32P_0/GCLK6		External I/O pin number Spartan-3 connection A8
21	GND		Ground
22	32N_0/GCLK7		External I/O pin number Spartan-3 connection B8
23	29N_0		" E7
24	29P_0		" D7
25	30N_0		" C7
26	30P_0		" B7
27	31N_0		" D8
28	31P_0/VREF0		" C8
29	IOa_1		" A9
30	IOb_1		" A12
31	IOc_1		" C10
32	IO/VREF1		" D12
33	01N_1/VRP_1		" A14
34	01P_1/VRN_1		" B14
35	10N_1/VREF1		" A13
36	10P_1		" B13
37	27N_1		" B12
38	27P_1		" C12
39	28N_1		" D11
40	28P_1		" E11
41	GND		Ground
42	GND		Ground
43	+3.3VIN		Power input +3.3V
44	+3.3VIN		Power input +3.3V

7.3. CON3 External I/O Connector

This JTAG connector is for external I/O or TE7720 (the connector is not mounted the board).

Table 7-3 External I/O Connector

No.	Signal Name	I/O	Function
1	+3.3VIN		Power input +3.3V
2	+3.3VIN		Power input +3.3V
3	GND		Ground
4	GND		Ground
5	29N_1		External I/O pin number Spartan-3 connection B11
6	29P_1		" C11
7	30N_1		" D10
8	30P_1		" E10
9	31N_1/VREF1		" A10
10	31P_1		" B10
11	01N_2/VRP_2		" B16
12	01P_2/VRN_2		" C16
13	16N_2		" C15
14	16P_2		" D14
15	17N_2		" D15
16	17P_2/VREF2		" D16
17	19N_2		" E13
18	19P_2		" E14
19	20N_2		" E15
20	20P_2		" E16
21	21N_2		" F12
22	21P_2		" F13
23	32N_1/GCLK5		" C9
24	GND		Ground
25	32P_1/GCLK4		External I/O pin number Spartan-3 connection D9
26	GND		Ground
27	22N_2		External I/O pin number Spartan-3 connection F14
28	22P_2		" F15
29	23N_2/VREF2		" G12
30	23P_2		" G13
31	24N_2		" G14
32	24P_2		" G15
33	39N_2		" H13
34	39P_2		" H14
35	40N_2		" H15
36	40P_2/VREF2		" H16
37	01N_3/VRP_3		" P16
38	01P_3/VRN_3		" R16
39	IOa_3		" K15
40	IOa_2		" G16
41			Unused
42	EXRESET*		No Connection (Caution: Do not input signals)
43	+3.3VOUT		Power output for internal logic +3.3V
44	GND		Ground

7.4. CON4 External I/O Connector

This is an external I/O connector (the connector is not mounted on the board).

Table 7-4 CON4 External I/O Connector

No.	Signal Name	I/O	Function
1			Unused
2			Unused
3	22N_3		External I/O pin number Spartan-3 connection L15
4	22P_3		L14
5	23N_3		K12
6	23P_3/VREF3		L12
7	24N_3		K14
8	24P_3		K13
9	39N_3		J14
10	39P_3		J13
11	40N_3/VREF3		J16
12	40P_3		K16

7.5. CON5 External I/O Connector

This is an external I/O connector (connector not mounted).

Table 7-5 CON5 External I/O Connector

No.	Signal Name	I/O	Function
1	GND		Ground
2	+3.3VOUT		Power output for internal logic +3.3V
3	16N_3		External I/O pin number Spartan-3 connection P15
4	16P_3		P14
5	17N_3		N16
6	17P_3/VREF3		N15
7	19N_3		M14
8	19P_3		N14
9	20N_3		M16
10	20P_3		M15
11	21N_3		L13
12	21P_3		M13

7.6. CON7 FPGA JTAG Connector

This is a JTAG connector for the FPGA (connector not mounted on the board).
It operates on +2.5V. Please use a JTAG cable compatible the +2.5V.

Table 7-6 CON7 JTAG Connector for Spartan-3

No.	Signal Name	I/O	Function 能
1	GND		Ground
2	+2.5VOUT		Power output for internal logic +2.5V
3	TCK	I	JTAG
4	TDI	I	JTAG
5	TDO	O	JTAG
6	TMS	I	JTAG

7.7. CON1 RS232C Connector

This is a RS232C connector that is connected to FPGA via Level Buffer.
Type and name of manufacturer of the connector used on the board is A1-10PA-2.54DSA/Hirose (or equivalents).

Serial Console Settings:

- Data Rate: 115.2kbps
- Data: 8bit
- Stop Bit: 1bit
- Flow Control: None

Table 7-7 CON1 RS232C Connector

No.	Signal Name	I/O	Function	
1			Unused	
2			Unused	
3	RXD	I	Spartan-3 connection pin number	E2 for serial console
4	RTS	O	“	F4
5	TXD	O	“	E4 for serial console
6	CTS	I	“	E1
7			Unused	
8			Unused	
9	GND		Ground	
10	+3.3VOUT		Power output for internal logic +3.3V	

7.8. JP1 Boot Mode Jumper

This jumper is used to sellect the boot mode.
If it is set to open, the board will go into auto boot mode.
If it is set to short, the board will go into boot loader mode.
The jumper is connected to FPGA.
For more information about the boot mode, refer to the software manual.

Table 7-8 JP1 Boot Mode Jumper

No.	Signal Name	I/O	Function
1	DLOAD		Open: Auto Boot Short: Boot Loader Mode Spartan-3 connection pin number F3
2	GND		Ground

7.9. JP2 FPGA Programming Jumper

This jumper is used to program configuration data to the Flash memory from the FPGA programming JTAG.
For jumper configuration, refer to “FPGA Configuration” in Section 10.

Table 7-9 JP2 FPGA Programming Jumper

No.	Signal Name	I/O	Function
1	TE77PRG		Open: Normal boot Short: Configuration data programming
2	GND		Ground

7.10. D3 Power-on LED

The LED lights (green) when the board is being fed 3.3V.

7.11. D1 User-Controlled LED

This LED can be user-controlled.
It lights at “LO.” level (red).
It is connected to the FPGA.

Table 7-10 D1 User-Controlled LED

No.	Signal Name	I/O	Function
	LED0		LO. Level: ON HI. Level: OFF Spartan-3 connection pin number G5

7.12. CON6 Power Input +3.3V Connector

This is the power input connector. “Power Input +3.3V must be +3.3V±3% and simple increment.
It is internally connected to the “power input +3.3V” at CON2 and CON3.
Type and name of manufacturer of the connector used on the board side is B2PS-VH/J.S.T. (or equivalent).
Type and name of manufacturer of the connector used on the cable side is Housing VHR-2N/J.S.T. (or equivalent), Contact BVH-21T-P1.1/J.S.T. (or equivalents) or BVH-41T-P1.1/J.S.T. (or equivalent).

Table 7-11 CON6 Power Input +3.3V Connector

No.	Signal Name	I/O	Function
1	GND		Ground
2	+3.3VIN		Power Input +3.3V

7.13. Ethernet 10/100 Base-T

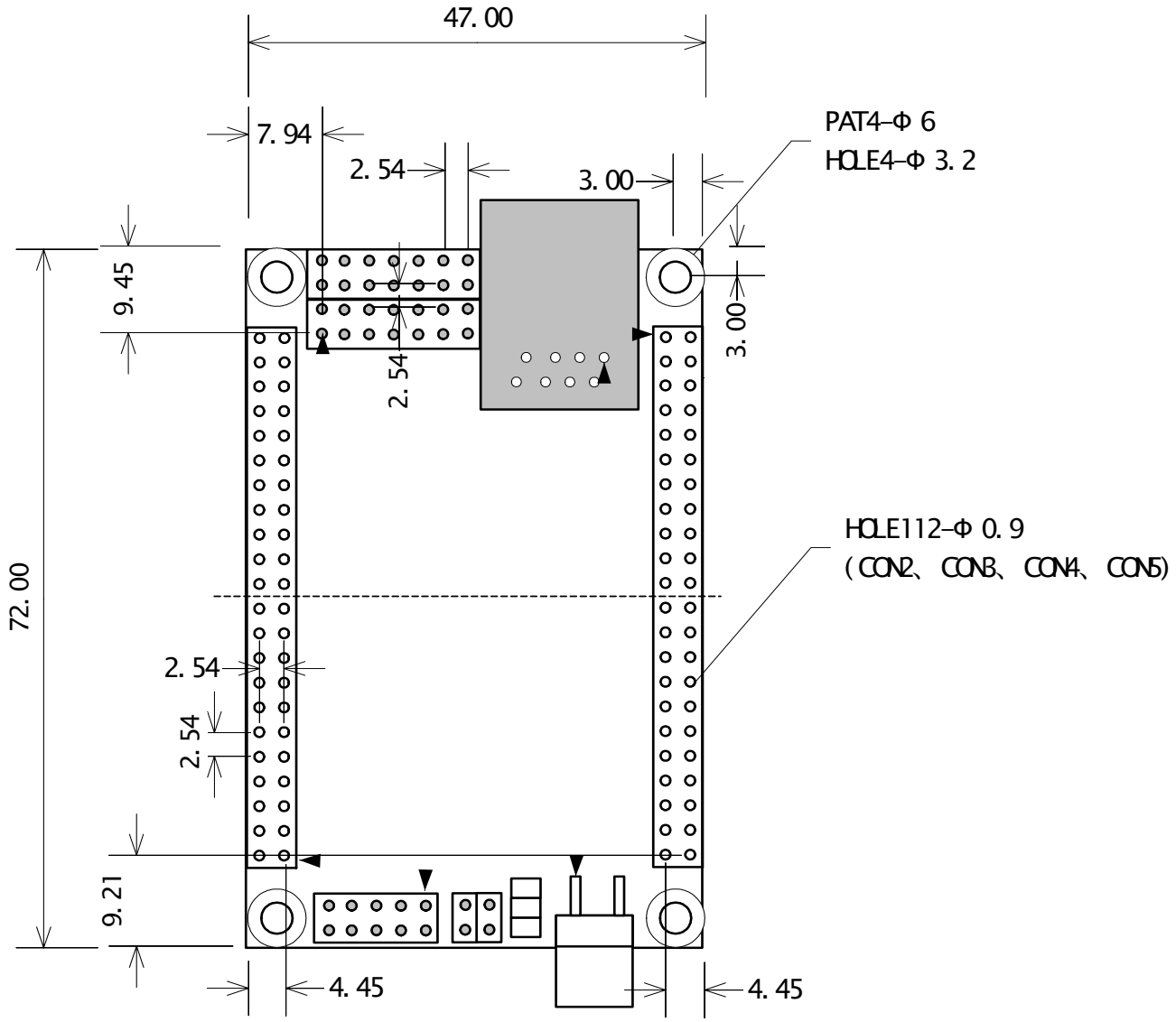
Type and name of manufacturer of the connector used on the board side is J0026D21B/PULSE.

Table 7-12 Ethernet 10/100 Base-T

No.	Signal Name	I/O	Function
1	TX+		Differential twist pair output+
2	TX-		Differential twist pair output -
3	RX+		Differential twist pair input+
4			75Ω termination (#4-pin and #5-pin are shorted).
5			75Ωtermination (#4-pin and #5-pin are shorted).
6	RX-		Differential twist pair input -
7			75Ω termination (#7-pin and #8-pin are shorted).
8			75Ωtermination (#7-pin and #8-pin are shorted).

8. Board Layout

The external view of this board is shown in **Figure 8-1**.



[unit: mm]

Figure 8-1 Board Layout of the SUZAKU

9. Revision History

Rev	Revision Date	Description of Change
1.0	2004/04/29	Initial Release
1.0.1	2004/06/04	・Correction to “SUZAKU Memory Map” at Section 5.1 Before: 0x00000000 – 0x00000FFF BRAM After: 0x00000000 – 0x00001FFF BRAM ・Correction to “Editing Project Top File” at Section 9.5 Before: ¥suzaku_v00¥xps_proj¥top.vhd After: ¥suzaku_v00¥top.vhd
1.0.2	2004/06/11	・Change of FPGA project folder name on CD-ROM ・Addition of installation of driver due to LBPLAY2 error. ・Addition of UART connection to a PC RS232C.
1.0.3	2004/06/16	・Addition of software reset.
1.0.4	2004/12/14	Updated company address Removed software related sections “9. Creating a FPGA Project” and “10. FPGA Configuration”.

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